Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Canceled)

2. (Currently Amended) A memory device as claimed in ~~claim 1~~claim 21, wherein the piezoelectric material is a ferroelectric material.

3. (Currently Amended) A memory device as claimed in ~~claim 1~~claim 21, wherein said first layer and said second layer are clamped together such as to enhance the amplitude of a voltage generated across one of the first and second layers due to the application of a voltage to the other of the first and second layers, the clamping together ~~is~~ being achieved by one of the following means: a means for maintaining a constant spacing between said ~~input~~ first and ~~output~~ third electrodes, and a means for exerting a constant force or stress upon one of the ~~input~~ first and ~~output~~ third electrodes relative to the other of the ~~input~~ first and ~~output~~ third electrodes.

4. (Currently Amended) A memory device as claimed in claim 2, wherein said first layer and said second layer are clamped together such as to enhance the amplitude of a voltage generated across one of the first and second layers due to the application of a voltage to the other of the first and second layers, said clamping together ~~is~~ being achieved by one of the following means: a means for maintaining a constant spacing between said ~~input~~ first and ~~output~~ third electrodes, and a means for exerting a constant force or stress upon one of the ~~input~~ first and ~~output~~ third electrodes relative to the other of the ~~input~~ first and ~~output~~ third electrodes.

5. (Canceled)

6. (Currently Amended) A memory ~~arrangement~~ device as claimed in ~~claim 5~~claim 2, wherein the respective ~~input~~ first electrodes are arranged parallel to each other in a

spaced apart manner in a first plane, the respective ~~common~~ second electrodes are arranged parallel to each other in a spaced apart manner in a second plane and the respective ~~output~~ third electrodes are arranged parallel to each other in a spaced apart manner in a third plane, with the ~~said~~ planes being parallel to each other, the ~~input~~ first and ~~output~~ third electrodes being parallel with each other and the ~~common~~ second electrodes being perpendicular ~~thereto~~ to the first and third electrodes.

7-16. (Canceled)

17. (Currently Amended) A memory ~~arrangement~~ device as claimed in ~~claim 12~~claim 3, wherein the respective ~~input~~ first electrodes are arranged parallel to each other in a spaced apart manner in a first plane, the respective ~~common~~ second electrodes are arranged parallel to each other in a spaced apart manner in a second plane and the respective ~~output~~ third electrodes are arranged parallel to each other in a spaced apart manner in a third plane, with the ~~said~~ planes being parallel to each other, the ~~input~~ first and ~~output~~ third electrodes being parallel with each other and the ~~common~~ second electrodes being perpendicular ~~thereto~~to the first and third electrodes.

18. (Currently Amended) A memory ~~arrangement~~ device as claimed in ~~claim 13~~claim 4, wherein the respective ~~input~~ first electrodes are arranged parallel to each other in a spaced apart manner in a first plane, the respective ~~common~~ second electrodes are arranged parallel to each other in a spaced apart manner in a second plane and the respective ~~output~~ third electrodes are arranged parallel to each other in a spaced apart manner in a third plane, with the ~~said~~ planes being parallel to each other, the ~~input~~ first and ~~output~~ third electrodes being parallel with each other and the ~~common~~ second electrodes being perpendicular ~~thereto~~to the first and third electrodes.

19. (Currently Amended) A memory ~~arrangement~~ device as claimed in ~~claim 14~~claim 21, wherein the respective ~~input~~ first electrodes are arranged parallel to each other in

a spaced apart manner in a first plane, the respective ~~common~~ second electrodes are arranged parallel to each other in a spaced apart manner in a second plane and the respective ~~output~~ third electrodes are arranged parallel to each other in a spaced apart manner in a third plane, with the ~~said~~ planes being parallel to each other, the ~~input~~ first and ~~output~~ third electrodes being parallel with each other and the ~~common~~ second electrodes being perpendicular ~~thereto~~to the first and third electrodes.

20. (Canceled)

21. (New) A memory device comprising:

a plurality of first electrodes;

a plurality of second electrodes;

a plurality of third electrodes;

a plurality of memory cells provided corresponding to intersections between the plurality of first electrodes and the plurality of second electrodes; and

a plurality of comparators each of which has a first input and a second input,

each of the plurality of memory cells including a first layer including a piezoelectric material and a second layer including a ferroelectric material,

one second electrode of the plurality of the second electrodes being provided between the first layer and the second layer,

the first layer and the second layer being provided between one first electrode of the plurality of first electrodes and one third electrode of the plurality of third electrodes,

the one first electrode being connected to the first input included in one comparator of the plurality of comparators, and

the one third electrode being connected to the second input included in the one comparator.

22. (New) A memory device as claimed in claim 21, wherein said one comparator compares a first signal between the one first electrode and the one second electrode with a second signal between the one third electrode and the one second electrode.